The Hong Kong University of Science and Technology

UG Course Syllabus

FPGA based Design: From Theory to Practice

4320

3 Credits

Prerequisite(s): ELEC 2350, or ELEC 3310

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Course Description

This course introduces the basic theory and design skills for FPGA-based design. The course aims to equip the students with enough knowledge and skills for the real word engineering using FPGA devices. Major topics include introduction to reconfigurable computing, hardware description language, RTL design and High-level synthesis, FPGA device, and mapping flow. Students will gain hands-on experiences of the complete FPGA based design cycle, from design specification, synthesis, implementation and simulation in this course.

Intended Learning Outcomes (ILOs)

By the end of this course, students should be able to:

1. Understand the basics of FPGA device and its mapping tool.

2. Learn the basics of Verilog language and be able to use Verilog for simple RTL design.

3. Understand the concept of High-Level Synthesis and its basic design flow.

Assessment and Grading

This course will be assessed using criterion-referencing and grades will not be assigned using a curve. Detailed rubrics for each assignment are provided below, outlining the criteria used for evaluation.

Assessments:

Assessment Task	Contribution to Overall Course grade (%)	Due date
Homework	20%	Every month
Lab report	20%	Every 3 weeks
Midterm Exam	30%	In class on Nov. 3rd
Course project	30%	In week 13th

* Assessment marks for individual assessed tasks will be released within two weeks of the due date.

Mapping of Course ILOs to Assessment Tasks

Assessed Task	Mapped ILOs	Explanation
Homework	ILO1, ILO2, ILO3	This task evaluates students' understanding of basic FPGA architecture and synthesis algorithms (ILO 1), as well as their ability to develop designs using Verilog and HLS (ILO 2 and ILO 3).
Labs	ILO2. ILO3	The labs provided students with the opportunity to practice Verilog and HLS-based designs and assess their understanding of these concepts.
Midterm Exam	ILO1, ILO2, ILO3	This task evaluates students' understanding of reconfigurable computing, FPGA device architecture, and mapping flow (ILO 1), as well as their design and coding skills for Verilog and HLS-based designs (ILO 2 and ILO 3).
Course project	ILO2, ILO3	This task evaluates students' hands-on ability to design relatively complex FPGA-based systems at the RTL or HLS level and to apply these designs in practical applications (ILO 2 and ILO 3).

Grading Rubrics

- **Homework and Midterm Exam**: Full marks will be awarded for completely correct solutions. For partially correct solutions, sub-marks will be given based on the individual steps of the solution. Late submissions will incur penalties based on the delay: 15% for less than half a day late, 30% for one day late, and 50% for two days late. Submissions over two days late will not be accepted.
- **Lab**: Grades will be assigned based on the completion of the lab and timely submission of the report. Late reports will incur penalties as stated above. One make-up lab may be arranged for special circumstances with prior approval.
- **Course Project**: Grading will be based on the project's complexity, the quality of the design, individual student workload, project presentation, and the final project report. Late submissions will incur penalties as outlined above.

Final Grade Descriptors:

Grades	Short Description	Elaboration on subject grading description
A	Excellent Performance	Demonstrates a comprehensive grasp of subject matter, expertise in problem-solving, and good creativity in developing complex/practical RTL or HLS based designs on FPGA. Finish all the tasks in high-quality.

B	Good Performance	Shows good knowledge and understanding of the main subject matter, competence in problem-solving, and the ability to analyze and evaluate issues. Displays high motivation to learn, finish most of the assignment and labs, doing ok at Midterm exam, and show the ability to develop simple but working FPGA based designs in the course project.
C	Satisfactory Performance	Possesses adequate knowledge of core subject matter, competence in dealing with familiar problems, and some capacity for analysis and critical thinking. Shows persistence and effort to finish some of the homework, and labs. Finish most of the course projects. Attend the mid-term exam and achieve not too low score.
D	Marginal Pass	Has threshold knowledge of core subject matter, potential to achieve key professional skills, and the ability to make basic judgments. Shows persistence and effort to finish some of the homework, and labs. Try the course project, and the project is partially finished. Attend the mid-term exams.
F	Fail	Demonstrates insufficient understanding of the subject matter and lacks the necessary problem-solving skills. Shows limited ability to think critically or analytically and exhibits minimal effort towards achieving learning goals, such as not submitting homework, missing labs, not attend the mid-term exam, etc.

Course AI Policy

AI may not be very helpful for the course. The student can use AI to search for course-related knowledge, but the student needs to determine the information is correct or not.

Communication and Feedback

Assessment marks for individual assessed tasks will be communicated via Canvas within two weeks of submission. Students who have further questions about the feedback including marks should consult the instructor within five working days after the feedback is received.

Resubmission Policy

We have penalty for late submission for homework, lab and course project.

Required Texts and Materials

Course materials in Canvas.

Academic Integrity

Students are expected to adhere to the university's academic integrity policy. Students are expected to uphold HKUST's Academic Honor Code and to maintain the highest standards of academic integrity. The University has zero tolerance of academic misconduct. Please refer to Academic Integrity | HKUST – Academic Registry for the University's definition of plagiarism and ways to avoid cheating and plagiarism.

Additional Resources

Online tutorials for RTL and HLS designs.