[ELEC4410] [CMOS VLSI Design] [Fall 2023] [Credits: 3]

Course Description

CMOS process and design rules; MOS device electronics; CMOS circuit and logic circuit characterization and performance estimation; VLSI design and verification tools. Laboratory work and the course project will be centered on industry standard tools using the commercial TSMC 180nm CMOS process.

List of Topics (according to Lecture days - Wednesdays)

Lecture Outline

Sep 6 - Lecture 1A - Introduction, Logistics, & Overview of CMOS VLSI Design
Sep 13 - Lecture 2 - MOS Transistor Theory, Part I: Basic Modeling & Operation
Sep 20 - Lecture 3 - MOS Transistor Theory, Part II: Second Order Modeling & Advanced Devices
Sep 27 - Lecture 4 - CMOS Fabrication, Layout, & IC Packaging

Oct 4 - Lecture 5 - CMOS Inverter: DC Characteristics
Oct 11 - Lecture 6 - CMOS Inverter: Dynamic Characteristics
Oct 18 - lecture 7 - Midterm Exam
Oct 25 - Lecture 8 - Power Consumption

Nov 1 - Lecture 9 - Combinational Logic Circuits & Logical Effort
Nov 8 - Lecture 10 - CMOS Logic Families
Nov 15 - Lecture 11 - Interconnect Analysis
Nov 22 - Lecture 12 - Introduction to Dynamic Logic Circuits
Nov 29 - Lecture 13 - Arithmetic Circuits

Laboratory Outline

Lab 1: UNIX Setup and Cadence Basics, Schematic Entry
Lab 2: Simulation with the Analog Design Environment
Lab 3: Hierarchical Schematic Design
Lab 4: Cadence Layout Tutorial
Lab 5: Layout Versus Schematic (LVS)
Lab 6: Post-Layout Simulation and Hierarchical Layout
Lab 7: Advanced Circuit Simulation Techniques

Intended Learning Outcomes:

On successful completion of this course, students will be able to:
CO1 – Recognize the advantages and critical importance of CMOS technology for very-large-scale integration.
CO2 – Understand the physical structure and operation of digital CMOS integrated circuits.
CO3 – Use a computer-aided-design tool for designing and characterizing CMOS integrated circuits.
CO4 – Design and demonstrate high-performance and compact digital CMOS integrated circuits.
CO5 – Understand the basic principles and current challenges in CMOS technology scaling.
CO6 – Foresee the evolution of the integrated circuits technology for the next 10+ years.
CO7 – Manage small-scale group projects.

CO8 – Demonstrate effective communication skills.
CO9 – Understand the professional and ethical responsibilities of engineers.

Textbook(s):

Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits – A Design Perspective, Second Edition, Prentice Hall, 2003.

Reference Books/Materials:

K. Martin, "Digital Integrated Circuit Design", Oxford, 2000.
K. Abbas, "Handbook of Digital CMOS Technology, Circuits, and Systems", Springer, 2020.
H. J. M. Veendrick, "Nanometer CMOS ICs: From Basics to ASICs", 2nd Ed., Springer, 2017.
N. H. E. Weste, D. M. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," 4th Ed., Addison Wesley, 2011.
S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits", 3rd Ed., Mc Graw Hill, 2003.
H. Kaeslin, "Digital Integrated Circuit Design From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
J. E. Ayers, "Digital Integrated Circuits: Analysis and Design," CRC Press, 2005.
I. E. Sutherland, B. F. Sproull, and D. L. Harris, "Logical Effort: Designing Fast CMOS Circuits," Morgan Kaufmann, 1998.

Relationship of Course to Program Outcomes:

Please refer to the Report Section 4.3.2 (iii).

Grading Scheme:

Project	21%
Laboratory	14%
Mid-Term Examination	25%
Final Examination	40%