ELEC4010O Practical Considerations of Analog Integrated Circuit Design
[Fall 2023] [Credits: 3]

Course Description

Properties of MOSFET are a strong function of its width and length due to short-channel effects. Even two MOSFETs with the same width and the same length, their properties are not identical due to process variations and various non-ideal effects such as layout dependent effects (LDEs) and parasitic elements in CMOS technology. In this course, students will learn about how the above mentioned effects affect analog circuit performance, and what kinds of methodologies can be used to minimize their impacts. *Prerequisite(s):* ELEC 3400

List of Topics

Lecture Outline

Week 1 Review of MOSFET DC Characteristics and AC Models
Week 2 MOSFET Layout View and Cross-Sectional View
Week 3 Short-Channel Effects and Layout-Dependent Effects
Week 4 Process Variations and Transistor Mismatch
Week 5 gm/id Design Methodology
Week 6 Matching of a Current Mirror
Week 7 Matching of a Differential Pair
Week 8 Offset Voltage of a Simple OTA
Week 9 Offset Voltage of a Current-Mirror OTA
Week 10 Offset Voltage of Folded-Cascode OTA
Week 11 Mismatch Reduction Techniques
Week 12 Parasitic Components in CMOS Technology
Week 13 Revision

Intended Learning Outcomes:

On successful completion of this course, students will be able to:

- Understand the layout view and cross-sectional view of PMOSFETs, NMOSFETs, and isolated-NMOSFETs.
- Identify parasitic components in CMOS technology and understand their impacts on analog circuits.
- Understand the impact of process variations, layout dependent effects, and short-channel effects, on analog circuits.
- Analyze and compute the impact of process variations on analog circuits such as accuracy of a current mirror and input offset voltage of an amplifier.
- Apply various design and layout methodologies to minimize the impact of process variations, layout dependent effects, and short-channel effects, on analog circuits.
- Apply industry software, Cadence, to design and simulate analog circuits under the impact of process variations, layout dependent effects, and short-channel effects.

Textbook(s):

Lecture notes will be available on the course webpage.

Reference Books/Materials:

Alan Hastings, *The Art of Analog Layout (2nd edition)*, Pearson Prentice Hall, 2006
Short Course from Prof. PE Allen
gm/id note from Prof. Bernhard Boser

Relationship of Course to Program Outcomes:

Please refer to the Report Section 4.3.2 (iii).

Grading Scheme:

Laboratory	30%
Project	40%
Final Examination	30%